METHOD FOR DETECTING LINE-TO-LINE FAULT LOCATION IN POWER NETWORK

BACKGROUND OF THE INVENTION

(a) Field of the invention

The present invention relates to a method for detecting a line-to-line fault location in power network, and more particularly, detecting the line-to-line fault location with direct 3-phase circuit analysis without using a symmetrical component transformation, whereby even in an unbalanced 3-phase circuit the line-to-line fault location can be accurately detected.

(b) Description of the Related Art

Rapid growth of economy has resulted in large scale of power systems, and an excessive increase in transmission and distribution networks of electric power systems causes many kinds of faults by various causes. Transmission and distribution networks of electric power systems are playing very important roles as the links between the power suppliers and the consumers. However, because most of lines are exposed to air, lightning, contact of animals or mal-functioning of protection devices causes many kinds of faults. When a line-to-line fault occurs, detecting a fault location rapidly and precisely separating the part of the network including the fault location from the rest part of the network until repairing the fault being finished is very important to minimize power interruption rate and to provide highly reliable power supplying service and electric power of high quality.

Transformation of 3-phase networks to symmetrical component systems (symmetrical component transformation) is generally used in conventional methods for detecting the line-to-line fault locations. A 3-phase balanced network can be transformed to a symmetrical

component system, which has no coupling between sequences so that the systems of equation may be solved easily. In other words, diagonal sequence impedance matrices are obtained in case of the balanced networks, thus sequence voltage and current can be expressed without any coupling among the sequences.

The advantage of the above method is that it can be easily applied to a balanced network. Zero sequence, positive sequence and negative sequence can be easily analyzed because they are not correlated, that is, there is no couplings, or equivalently, mutual impedances among the sequences.

However, the above conventional method can only be applied to a balanced network, because the simplified equations of zero sequence, positive sequence and negative sequence, which are not correlated, can be obtained by symmetrical component transformation only in the balanced network. Thus, the conventional method is not available for unbalanced systems.

SUMMARY OF THE INVENTION

The present invention has been made in an effort to solve the above problems.

It is an object of the present invention to provide a method for detecting a line-to-line fault location in a power network including a fault resistance, not using the symmetrical component transformation but using direct 3-phase circuit analysis. The line-to-line fault location detecting method of the present invention requires phase voltage and phase current of a fundamental frequency measured at a relay.

In the method using direct 3-phase circuit analysis of the present invention, matrix inverse lemma is applied to simplify matrix inversion calculations, thus the line-to-line fault location can be easily and accurately determined even in the case of an unbalanced network without using the symmetrical component transformation.

By using the method of the present invention, the line-to-line fault location can be directly analyzed whether the 3-phase network is balanced or unbalanced.

To achieve the above object, the present invention provides a method for detecting a line-to-line fault location in a power network comprising the steps of:

determining elements of a line impedance matrix and a load impedance matrix, and phase voltages and currents at a relay;

determining a line-to-line fault distance d by substituting said elements of said line impedance matrix and said load impedance matrix, and said phase voltage and current into a fault location equation based on direct circuit analysis;

wherein said fault location equation is derived from a model consisting of said phase voltage and current at the relay, a fault current, a fault resistance and the line-to-line fault distance;

wherein the model is based on the line-to-line fault between a-phase and b-phase and described by a model equation:

$$V_{Sa} - V_{Sb} = (1-d)((Zl_{aa} - Zl_{ba})I_{Sa} + (Zl_{ab} - Zl_{bb})I_{Sb} + (Zl_{ac} - Zl_{cb})I_{Sc}) + I_f R_f,$$

where, $V_{Sabc} = [V_{Sa} \quad V_{Sb} \quad V_{Sc}]'$: phase voltage vector, $I_{Sabc} = [I_{Sa} \quad I_{Sb} \quad I_{Sc}]'$: phase current vector, $Zl_{abc} = \begin{bmatrix} Zl_{aa} & Zl_{ab} & Zl_{ac} \\ Zl_{ba} & Zl_{bb} & Zl_{bc} \\ Zl_{ca} & Zl_{cb} & Zl_{cc} \end{bmatrix}$: line impedance matrix, I_f: fault current, 1-d: fault distance;

wherein said fault location equation is derived by using the matrix inverse lemma: $(A^{-1} + BCD)^{-1} = A - AB(C^{-1} + DAB)^{-1}DA$, to simplify an inverse matrix calculation; and

wherein the fault location equation is derived by direct circuit analysis without using the conventional symmetrical component transformation method.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principles of the invention.

Fig. 1 shows a simple diagram of a line-to-line fault occurred in a general 3-phase power network whether it is balanced or unbalanced one;

Fig. 2 shows a flow of a preferred embodiment of the present invention;

Fig. 3 shows an example of the unbalanced system where a line-to-line fault between a-phase and b-phase occurs;

Fig. 4 shows errors resulted by using conventional method in case of line-to-line fault for the unbalanced system; and

Fig. 5 shows errors resulted by using the proposed method in the same case as in Fig. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiment of the present invention will now be described in detail, with reference to the accompanying drawings.

Fig. 1 shows general 3-phase transmission and distribution of simplified diagram of faulted network whether they are operated in a balance or unbalance manner. The proposed algorithm use voltages and currents measured at a relay.

Based on a model shown in Fig. 1 and assuming the capacitance of lines negligible, phase voltages and phase currents at the location of relay A satisfy the following model equation.

$$V_{Sa} - V_{Sb} = (1-d)((Zl_{aa} - Zl_{ba})I_{Sa} + (Zl_{ab} - Zl_{bb})I_{Sb} + (Zl_{ac} - Zl_{cb})I_{Sc}) + I_f R_f \qquad (1)$$

Where, V_{Sa} and V_{Sb} are phase voltages of a-phase and b-phase respectively, and I_{Sa}, I_{Sb}

and I_{Sc} are phase currents of a-phase, b-phase and c-phase respectively at the relay A, $I_{Sabc} = [I_{Sa} \quad I_{Sb} \quad I_{Sc}]^T$ is a phase current vector at the relay A, $Zl_{abc} = \begin{bmatrix} Zl_{aa} & Zl_{ab} & Zl_{ac} \\ Zl_{ba} & Zl_{bb} & Zl_{bc} \\ Zl_{ca} & Zl_{cb} & Zl_{cc} \end{bmatrix}$ represents a line impedance matrix, I_f represents a fault current, R_f is a fault resistance, d is a fault distance.

In equation (1), the line impedance is given, and the phase voltages and currents at relay can be measured. However, the fault current I_f and fault resistance R_f are unknown. They can be obtained using the direct 3-phase circuit analysis of this invention as described below.

The fault current I_f can be represented as a function of the phase currents at the relay using current distribution law of a parallel admittance network:

$$\begin{bmatrix} I_f \\ 0 \\ 0 \end{bmatrix} = Y_f [Y_f + (dZl_{abc} + Zr_{abc})^{-1}]^{-1} \begin{bmatrix} I_{Sa} \\ I_{Sb} \\ I_{Sc} \end{bmatrix} \qquad (2)$$

where, $Y_f = \begin{bmatrix} 1/R_f & -1/R_f & 0 \\ -1/R_f & 1/R_f & 0 \\ 0 & 0 & 0 \end{bmatrix}$: the fault admittance matrix at the fault location; and

$Zr_{abc} = \begin{bmatrix} Zr_{aa} & Zr_{ab} & Zr_{ac} \\ Zr_{ba} & Zr_{bb} & Zr_{bc} \\ Zr_{ca} & Zr_{cb} & Zr_{cc} \end{bmatrix}$: the load impedance matrix.

The inverse matrix $[Y_f + (dZl_{abc} + Zr_{abc})^{-1}]^{-1}$ in Eq. (2) can be simplified by the matrix inverse lemma:

$$(A^{-1} + BCD)^{-1} = A - AB(C^{-1} + DAB)^{-1} DA \qquad (3)$$

A, B, C and D are defined as follows:

$$A \equiv (dZl + Zr) = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \qquad (4)$$

$$B \equiv \begin{bmatrix} 1 \\ -1 \\ 0 \end{bmatrix}, \quad C \equiv 1/R_f, \quad D \equiv [1 \quad -1 \quad 0] \qquad (5)$$

Then, applying the lemma, we obtain:

$$[Y_f + (dZl + Zr)^{-1}]^{-1} =$$

$$\begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} - \begin{bmatrix} a_{11} - a_{12} \\ a_{21} - a_{22} \\ a_{31} - a_{32} \end{bmatrix} (R_f + a_{11} + a_{22} - a_{12} - a_{21})^{-1} [a_{11} - a_{21} \quad a_{12} - a_{22} \quad a_{13} - a_{23}] =$$

$$\begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} - \frac{1}{(R_f + a_{11} + a_{22} - a_{12} - a_{21})} \times$$

$$\begin{bmatrix} (a_{11} - a_{12})(a_{11} - a_{21}), & (a_{11} - a_{12})(a_{12} - a_{22}), & (a_{11} - a_{12})(a_{13} - a_{23}) \\ (a_{21} - a_{22})(a_{11} - a_{21}), & (a_{21} - a_{22})(a_{12} - a_{22}), & (a_{21} - a_{22})(a_{13} - a_{23}) \\ xx & xx & xx \end{bmatrix} =$$

$$\frac{1}{(R_f + a_{11} + a_{22} - a_{12} - a_{21})} \times$$

$$\begin{bmatrix} (R_f a_{11} + a_{11}a_{22} - a_{12}a_{21}), & (R_f a_{12} + a_{11}a_{22} - a_{21}a_{12}), & (R_f a_{13} + a_{22}a_{13} - a_{21}a_{13} + a_{23}a_{11} - a_{23}a_{12}) \\ (R_f a_{21} + a_{11}a_{22} - a_{12}a_{21}), & (R_f + a_{11}a_{22} - a_{12}a_{21}), & (R_f a_{23} + a_{11}a_{23} - a_{12}a_{23} - a_{13}a_{21} + a_{13}a_{22}) \\ xx & xx & xx \end{bmatrix} \qquad (6)$$

Then the fault current equation, Eq.(2) can be rewritten as:

$$\begin{bmatrix} I_f \\ 0 \\ 0 \end{bmatrix} = \frac{1}{(R_f + C_1 - C_2)} \begin{bmatrix} C_1 & C_2 & C_3 \\ xx & xx & xx \\ xx & xx & xx \end{bmatrix} \begin{bmatrix} I_{Sa} \\ I_{Sb} \\ I_{Sc} \end{bmatrix} \qquad (7)$$

where, xx represents an element that we have no concern and other coefficients are as follows:

$C_1 = a_{11} - a_{21} = d(Zl_{aa} - Zl_{ba}) + Zr_{aa} - Zr_{ba} = dA_1 + B_1$,

$C_2 = a_{12} - a_{22} = d(Zl_{ab} - Zl_{bb}) + Zr_{ab} - Zr_{bb} = dA_2 + B_2$ and

$C_3 = a_{13} - a_{23} = d(Zl_{ac} - Zl_{bc}) + Zr_{ac} - Zr_{bc} = dA_3 + B_3$. (8)

Thus, the final expression for the fault current becomes:

$$I_f = \frac{C_1 I_{Sa} + C_2 I_{Sb} + C_3 I_{Sc}}{(R_f + C_1 - C_2)} \qquad (9)$$

Substitution of Eq. (9) into the model equation of Eq. (1) and rearrangement can make a second order polynomial with respect to the distance variable d using expressions of the coefficients as in Eq. (8).

$$d^2(a_r + ja_i) + d(b_r + jb_i) + c_r + jc_i + R_f(d_r + jd_i) = 0 \qquad (10)$$

where, $a_r + ja_i = (A_1 - A_2)D_1$,

$b_r + jb_i = (A_1 - A_2)(V_{Sa} - V_{Sb} - D_1) + (B_1 - B_2)D_1$,

$c_r + jc_i = (B_1 - B_2)(V_{Sa} - V_{Sb} - D_1)$,

$d_r + jd_i = (V_{Sa} - V_{Sb} - D_1 - D_2)$,

$D_1 = A_1 I_{Sa} + A_2 I_{Sb} + A_3 I_{Sc}$ and

$D_2 = B_1 I_{Sa} + B_2 I_{Sb} + B_3 I_{Sc}$. (11)

From the imaginary part of Eq. (10), the following second order polynomial equation can be obtained.

$$d^2(a_r - \frac{d_r}{d_i}a_i) + d(b_r - \frac{d_r}{d_i}b_i) + c_r - \frac{d_r}{d_i}c_i = 0 \qquad (12)$$

Finally the fault distance d can be obtained by solving Eq. (12). Note that this fault location equation based on the direct circuit analysis can be applied to any system, which is balanced or unbalanced type, three phase or three/single phase systems.

Fig. 2 shows a flow chart of the preferred embodiment of this invention.

The preferred embodiment shown in Fig. 2 comprises the steps of: determining elements of a line impedance matrix and a load impedance matrix, and phase voltages and currents at a relay (step S10); determining a line-to-line fault distance d by substituting said elements of said line impedance matrix and said load impedance matrix, and said phase voltages and currents into a fault location equation based on direct circuit analysis (step S20); and outputting the line-to-line fault distance d to the network protecting device such as

protective relays (step S30).

The suggested method based on direct circuit analysis for the line-to-line fault has been also applied to the unbalanced system in Fig. 3 for verification. The line-to-line fault is assumed to have occurred between A and B. The results are compared with those of the conventional method using the distribution factor. Fig. 4 shows errors resulted by using the conventional method in case of line-to-line fault for the unbalanced system, while the Fig. 5 shows errors resulted by using the proposed method in the same case as in Fig. 4.

A significant accuracy difference can be observed between two results. The maximum estimation error is 8% in case of the conventional method while 0.15% in case of the proposed method. The error in the proposed method is very small showing its effectiveness for the real application.

A new fault location algorithms based on the direct circuit analysis are suggested. Application of the matrix inverse lemma has greatly simplified the derivation of the fault location equations that, otherwise, are too complicated to be derived. The proposed algorithms overcome the limit of the conventional fault location algorithms based on the sequence circuit analysis, which assumes the balanced system requirement. The proposed algorithms are applicable to any power system, but especially useful for the unbalanced distribution systems. Its effectiveness has been proved through many EMTP simulations.

The objective of the embodiments and drawings is to clearly explain the present invention and does not limit the technical scope of the invention. The present invention described above can be replaced, modified and changed by one skilled in the art, as long as such changes do not exceed the technical scope of the invention. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.